

## **IC Layout Designer**

HONG KONG OR SHENZHEN, FULL-TIME REGULAR

IC layout designer will be responsible for layout of cutting edge high-speed high-performance CMOS integrated circuits in deep submicron CMOS processes such as 28nm HPC, 16nm FF+/FFC etc.

### **Qualifications**

- 3 years of work experience in high-performance analog/mixed-signal IC layout in deep submicron CMOS processes
- Extensive experience with layout of high-performance analog blocks such as analog-to-digital converter, digital-to-analog converter, PLL and precision reference
- Strong understanding of high-performance analog layout techniques such as common centroid layout, use of dummies, shielding, full of symmetry, thermal aware layout, and layout consideration for electromigration, substrate noise
- Familiar with skill code and layout automation
- Must be able to work independently according to schedules and be team player
- Strong written and verbal communication skills